

CLAIMS

1 1. A semiconductor device having a self-aligned contact, the semiconductor
2 device comprising:

3 a plurality of conductive patterns formed to be adjacent to one another by
4 sequentially stacking and patterning a first conductive layer and a mask layer on a
5 particular underlying layer;

6 a first insulation layer filling a gap between adjacent conductive layer patterns
7 such that the upper portion of each conductive layer pattern is exposed;

8 a second insulation layer having a spacer shape, the second insulation layer
9 formed on the sides of each conductive layer pattern exposed above the first insulation
10 layer; and

11 a second conductive layer filling a contact hole which is self-aligned with respect
12 to the second insulation layers between adjacent conductive layer patterns and which
13 passes through the first insulation layer.

1 2. The semiconductor device of claim 1, wherein the top of the first insulation
2 layer is lower than the top of the first conductive layer of each conductive layer pattern.

1 3. The semiconductor device of claim 1, wherein the top of the first insulation
2 layer is higher than the top of the first conductive layer of each conductive layer pattern.

1 4. The semiconductor device of claim 1, wherein an etching rate of the first
2 insulation layer is larger than that of the second insulation layer.

1 5. The semiconductor device of claim 1, wherein the dielectric constant of
2 the first insulation layer is smaller than that of the second insulation layer.

1 6. The semiconductor device of claim 1, wherein the first insulation layer is
2 formed of a silicon oxide layer.

1 7. The semiconductor device of claim 1, wherein the second insulation layer
2 is formed of a silicon nitride layer.

1 8. The semiconductor device of claim 1, further comprising a third insulation
2 layer provided between the first insulation layer and the sides of each conductive layer
3 pattern and between the second insulation layer and the side of the conductive layer
4 pattern.

1 9. The semiconductor device of claim 8, wherein the third insulation layer is
2 formed of a silicon nitride layer to a thickness of 50-200 Å.

1 10. The semiconductor device of claim 1, further comprising a fourth
2 insulation layer provided on the surface of the underlying layer except for a portion
3 contacting the second conductive layer and on the surfaces of the conductive layer
4 patterns.

1 11. The semiconductor device of claim 10, wherein the fourth insulation layer
2 is formed of a silicon nitride layer to a thickness of 50-200 Å.

1 12. The semiconductor device of claim 11, further comprising a field oxide
2 layer formed on a certain portion of the surface of the underlying layer, wherein the
3 second conductive layer is formed to at least partially contact the field oxide layer.

1 13. The semiconductor device of claim 11, further comprising a conductive
2 pad layer formed on a certain portion of the surface of the underlying layer, wherein the
3 second conductive layer is formed to contact the surface of the conductive pad layer.

1 14. The semiconductor device of claim 1, wherein the first conductive layer of
2 each conductive layer pattern is a bit line, and the second conductive layer serves to

3 connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

1 15. The semiconductor device of claim 1, wherein the first conductive layer of
2 each conductive layer pattern is a gate electrode, and the contact contacts the surface
3 of a semiconductor substrate.

1 16. A method for fabricating a semiconductor device having a self-aligned
2 contact, the method comprising:

3 forming a plurality of conductive layer patterns adjacent to one another by
4 sequentially stacking a first conductive layer and a mask layer on a particular underlying
5 layer and patterning the first conductive layer and the mask layer;

6 filling a gap between adjacent conductive layer patterns by depositing a first
7 insulation layer on the surface of the underlying layer on which the conductive layer
8 patterns are formed;

9 etching the entire surface of the first insulation layer to expose the upper portion
10 of each conductive layer pattern;

11 forming a spacer of a second insulation layer on the sides of each exposed
12 conductive layer pattern;

13 forming a contact hole self-aligned with respect to spacers so that the surface of
14 the underlying layer between adjacent conductive layer patterns is exposed; and

15 forming a second conductive layer by filling the contact hole with a conductive
16 material.

1 17. The method of claim 16, further comprising planarizing the surface of the
2 first insulation layer after filling the gap between the adjacent conductive layer patterns
3 with the first insulation layer.

1 18. The method of claim 16, further comprising forming an interlayer
2 insulation layer, the surface of which is planarized, on the entire surface of the resultant
3 structure obtained after forming the spacer of the second insulation layer.

1 19. The method of claim 16, further comprising forming an insulation layer
2 used as an etching stopper on the entire surface of the resultant structure obtained
3 after forming the conductive layer patterns.

1 20. The method of claim 19, further comprising forming a spacer of the
2 insulation layer used as the etching stopper on the sides of each conductive layer
3 pattern by etching the insulation layer used as the etching stopper.